

**AMENDMENTS TO THE SPECIFICATION**

Please replace the paragraphs beginning on page 3, line 23 as shown below:

Fig. [[2]] 2A-2J illustrates the variation in time of control and output signals at certain nodes of the circuit of Fig. 1 during precharge operations; and

Fig. [[3]] 3A-3L illustrates the variation with time of control and output signals at certain nodes of the circuit of Fig. 1 during the reading of a datum.

Please replace the paragraph beginning on page 6, line 7 as shown below:

The drain of transistor P24 is connected to a second high supply rail  $[[V_{cc}]]$  VRS, the voltage level of which is, according to the present invention, greater than the write levels of storage elements 2 and to the precharge level of amplifier SA. In the considered case, the highest write level and the precharge level of amplifier SA are equal to the voltage of first high supply rail  $[[V_{dd}]]$  VRS. The gate of transistor P24 receives a refreshment control signal RESTORE.

Please replace the paragraph beginning on page 11, line 7 as shown below:

The space gain and the simplification of memory device manufacturing methods widely compensates for the use of high-voltage dual-gate transistors, especially for transfer stage 3 and precharge stage 16, which must be able to stand in the off state a relatively high refreshment voltage  $[[V_{cc}]]$  VRS.